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(54) Quantization of input vectors with and without rearrangement of vector elements of a candidate vector.

(57) For quantizing input vectors into output codes with reference to quantization vectors with reduction of a memory capacity, a vector quantizer device comprises a rearranging unit (21, 23) between a codebook circuit (17) preliminarily loaded, in accordance with codebook indexes, with code vectors selected from the quantization vectors to produce at least one candidate vector in response to a current index and a distance calculator (15) for calculating, between each input vector and comparison vectors given by the candidade vector, distance values for supply to an evaluation circuit (19) for producing a selected index indicative of one of the comparison vectors that minimizes the distance values and for successively producing the output codes with the selected index used as each output code without or with addition of a rearrangement index. When the rearrangement index is and is not added, the rearranging circuit produces the candidate vector in each comparison vector as an unchanged vector and as a rearranged vector in which vector elements of the candidate vector are rearranged, respectively. The rearranging unit may rearrange the candidate vector in compliance with a single predetermined rule or with rules preliminarily stored in a rearrangement table circuit (23) in accordance with table indexes with one of the rules delivered to a rearranging circuit (21) in response to the rearrangement index.

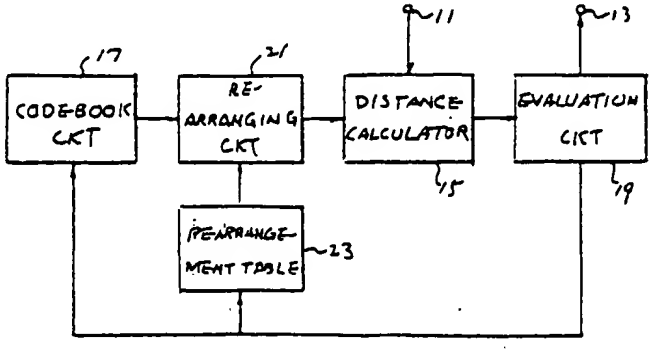

FIG. 2

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In accordance with an aspect of this invention, there is provided a vector quantizing method which is for quantizing input vectors into output codes and comprises the steps of preparing a codebook circuit loaded with code vectors in accordance with codebook indexes with each code vector composed of a predetermined number of vector elements, producing at least one candidate vector of the code vectors in response to a current index selected from the codebook indexes for each input vector, calculating distances between the above-mentioned each of input vectors and comparison vectors given by the at least one candidate vector to produce distance values representative of the distances, and evaluating the distance values to select one of the comparison vectors as a selected vector that minimizes the distance values, the evaluating step producing a selected index indicative of the selected vector to successively produce the output codes with the selected index used as each output code, wherein the vector quantizing method comprises the step of using in the comparison vectors the at least one candidate vector as an unchanged vector without rearrangement of its vector elements and the at least one candicate vector as a rearranged vector with rearrangement of its vector elements in response to a rearrangement index, the evaluating step producing the selected index with no change of and with addition of the rearrangement index to the current index when the selected vector is the unchanged and the rearranged vectors, respectively.

In accordance with a different aspect of this invention, there is provided a vector quantizer device which is for quantizing input vectors into output codes and comprises a codebook circuit preliminarily loaded with code vectors in accordance with codebook indexes with each code vector composed of a predetermined number of vector elements to produce at least one candidate vector of the code vectors in response to a current index selected from the codebook indexes for each of the input vectors, a distance calculator for calculating distances between the above-mentioned each of input vectors and comparison vectors given by the at least one candidate vector to produce distance values representative of the distances, and an evaluation circuit for evaluating the distance values to select one of the comparison vectors an a selected vector that minimizes the distance values, the evaluation circuit producing a selected index indicative of the selected vector to successively produce the output codes with the selected index used as each output code, wherein the vector quantizer device comprises vector rearranging means between the codebook circuit and the distance calculator for using in the comparison vectors the at least one candidate vector as an unchanged vector without rearrangement of its vector elements and the at least one candidate vector as a rearranged vector with rearrangement of its vector elements in response to a rearrangement index, the evaluation circuit producing the selected index with no change of and with addition of the rearrangement index to the current index when the selected vector is the unchanged and the rearranged vectors, respectively.

BRIEF DESCRIPTION OF THE DRAWING:

Fig. 1 is a block diagram of a conventional vector quantizer device;

Fig. 2 is a block diagram of a vector quantizer device according to a first embodiment of the instant invention;

Fig. 3 is a block diagram of a vector quantizer device according to a second embodiment of this invention;

Fig. 4 is a block diagram of a vector quantizer device according to a third embodiment of this invention;

Fig. 5 is a block diagram of a vector quantizer device according to a fourth embbdiment of this invention; and

Fig. 6 is a block diagram of a vector quantizer device according to a fifth embodiment of this invention.

DESCRIPTION OF THE PREFERRED EMBODIMENTS:

Referring to Fig. 1, a conventional vector quantizer device will first be described in order to facilitate an understanding of the present invention. Such a vector quantizer device is known in the art and is for quantizing a device input signal representative of input vectors into a device output signal indicative of output codes.

In Fig. 1, the vector quantizer device has a device input terminal 11 supplied with the device input signal and a device output terminal 13 to which the vector quantizer device produces the device output signal. From the device input terminal 11, the input vectors are delivered to a distance calculator 15 to which a codebook circuit 17 supplies from codebook code vectors prelminarily stored therein in accordance with codebook indexes several candidate vectors in response to a current index selected from the codebook indexes for each input vector in the manner which will presently be described. The codebook indexes specify the codebook code vectors, respectively. Several of the codebook code vectors are therefore

unchanged vector without rearrangement of the vector elements of this candidate vector. In such a manner, the rearranging circuit 21 supplies the distance calculator 15 with at least two comparison vectors for each input vector. In other words, such comparison vectors are delivered to the distance calculator 15 for the input vectors as the unchanged vectors and/or as the rearranged vectors.

It should be noted in this connection that the codebook circuit 17 produces at least one candidate vector in response to the current index. The rearranging circuit 21 produces either an unchanged or a rearranged vector for each candidate vector. It will nevertheless be said that either an unchanged or a rearranged vector is delivered in the comparison vectors to the distance calculator 15 for the at least one candidate vector.

For use in quantizing various input vectors by the vector quantizer device being illustrated, code vectors will now be referred to as quantization code vectors or simply as quantization vectors. It will be presumed as above that S quantization vectors C(s, n) should be used and that a first number S(1) of the quantization vectors are for use in the comparison vectors as the unchanged vectors with a second number S(2) of the quantization vectors used as the rearranged vectors.

Under the circumstances, the codebook circuit 17 must have a codebook memory capacity of S(1)N. If the rearranged vectors of a set should be produced by the rearranging circuit 21 in respective or individual manners of rearrangement, the rearrangement table circuit 23 must have a table memory capicity of S(2)N. The vector quantizer device must accordingly have a total memory capacity of SN and is not different from the memory capacity of a conventional case illustrated with reference to Fig. 1.

The manners of rearrangement are consequently selected in the example being illustrated as common manners so as to be common for candidate vectors which the codebook circuit 17 produces at least from predetermined ones of the codebook code vectors. It is thereby possible to reduce the manners of rearrangement to D in number for the common manners, where D is less than the second number. The total memory capacity becomes equal to (S(1) + D)N with a reduction of (S(2) - D)N as compared with the conventional case.

The vector quantizer device of Fig. 2 is different from the conventional vector quantizer device illustrated with reference to Fig. 1 in that the codebook code vectors comprise in the codebook circuit 17 the predetermined ones of quantization vectors for use by the table dependent rearranging circuit 21 either as the unchanged vectors or as the rearranged vectors and that the common manners of rearrangement are selected in common to respective or individual parts of the predetermined ones and are preliminarily stored in the rearrangement table circuit 23. The codebook code vectors may or may not include other code vectors other than the predetermined ones. If included, these other code vectors are used in the comparison vectors solely as the unchanged vectors. Each of the common manners is common to a part of the predetermined ones and is specified among the table indexes by the rearrangement index. Being at least a part of the codebook code vectors, the predetermined ones are specifed by at least a part of the codebook indexes.

Referring to Fig. 3, the description will proceed to a vector quantizer device according to a second embodiment of this invention. Similar parts are designated by like rerference numerals and are similarly operable with likewise named signals and quantities.

A single rule rearranging or reordering circuit 25 is substituted for a combination of the table dependent rearranging circuit 21 and the rearrangement table circuit 23 described in conjunction with Fig. 2. From the evaluation circuit 19, the command is delivered directly to the single rule rearranging circuit 25 so that the single rule rearranging circuit 25 should or should not rearrange the at least one candidate vector into the rearranged vector in compliance with a single predetermined rule which will presently be exemplified. In other words, the single rule rearranging circuit 25 produces the at least one candidate vector in the comparison vectors either as the unchanged vector or as the rearranged vector in compliance with a predetermined manner alone.

In Fig. 3, rearrangement of the candidate vector or vectors is carried out in the single manner. The total memory capacity is therefore rendered equal to S(1)N and is S(2)N less than the conventional case.

The single rule may, for example, to rearrange the vector elements of each candidate vector in a completely inverted order. More particularly, let one of the codebook code vectors be C(s(1), n) where s(1) is variable between 1 and the first number, both inclusive, n representing the vector elements numbered consecutively from 1 to N in the ascending order as described before. In this event, the rearranged vector is an order inverted vector C(s(2), j), where s(2) is variable between 1 and the second number, both inclusive, j representing the vector elements N, (N - 1), ..., 2, and 1 of the above-mentioned one of the codebook code vectors, which vector elements are consecutively numbered from N to 1 in a descending order, That is:

$$C(s(2), j) = C(s(2), N - n + 1). \quad (2)$$

Under the circumstances. the codebook circuit 17 is loaded with the codebook code vectors, each representative of the succession of a consonant and a vowel. For such sequential successions specified by the table indexes, the table indexes specify the common manners in which the succession of a consonant and a vowel in each candidate vector is rearranged into the succession of these vowel and consonant. When supplied with the mode zero and one signals, the rearrangement table circuit 23 is quiescent and is active to make the table dependent rearranging circuit 21 produce each candidate vector in the comparison vectors as the unchanged vector and as the rearranged vector. At any rate, use of the results of analysis exempts in general the distance calculator 15 from calculation of the distance values unless the inppt vector analyzer 27 produces the mode zero and the mode one signals.

Whether each input vector represents the succession of a consonant and a vowel or of a vowel and a consonant, is judged by the input vector analyzer 27 operable based on, for example, an article contributed by Erdal Paksoy and two others to the IEEE Proc. ICASSP - 93 (1994), pages II-155 to II-158, under the title of "Variable Rate Speech Coding with Phonetic Segmentation". When the mode zero signal is produced for a part, S(2) in number, of different Input vectors S in number, the vector quantizer device of Fig. 4 makes it possible to reduce the total memory capacity to S(1)N and by S(2)N less as compared with the conventional case. Furthermore, the amount of calculation by the distance calculator 15 is reduced by S(2) times.

Turning to Fig. 5, a vector quantizer device is according to a fourth embodiment of this invention. Similar parts are again designated by like reference numerals and are similarly operable with likewise named signals and quantities.

In Fig. 5, a table training circuit 29 is added to the vector quantizer device illustrated with reference to Fig. 2. The table training circuit 29 is connected to the rearrangement table circuit 23 and to a training input terminal 31 supplied with a plurality of training vectors which include various input vectors supplied to the device input terminal 11.

Before actual quantization of such various input vectors, the rearrangement table circuit 23 is trained by the training vectors so that the vector quantizer device ray have a highest possible quantization capability. More particularly, the table training circuit 29 produces in effect a plurality of rearrangement table circuits, such as 23. From these rearrangement table circuits, one is selected for actual use as the rearrangement table circuit 23 that attains the highest quantization capability. Mere use of a small memory capacity nay adversely affect the quantization capability. Additional use of the table training circuit 29 well compensates for a possible deterioration in the quantization capability.

Further turning to Fig. 6, a vector quantizer device is according to a fifth embodiment of this invention. Similar parts are designated by like reference numerals and are similarly operable with likewise named signals and quantities.

In Fig. 6, a rule training circuit 33 is added to the vector quantizer device of Fig. 3. The rule training circuit 33 is connected to the single rule rearranging circuit 25 and to the training input terminal 31.

Before actual quantization of various input vectors, operation of the single predetermined rule is trained in the rearranging circuit 25 by the training vectors to raise the quantization capability of the vector quantizer device. More specifically, various rules are provided by the rule training circuit 33. One of these rules is used as the single predetermined rule that achieves the highest quantization capability. Training of the rule is preferred like training of the rearrangement table circuit 23.

While this invention has thus far been described in specific conjunction with several preferred embodiments thereof, it will now be readily possible for one skilled in the art to put this invention into effect in various other manners. For example, use of the vector quantizer device is not limited to quantization of a speech signal into the output codes of a low bit rate. Above all, it is possible to use similarity measures instead of the distances in the manner known In the art. In this event, maximization should be used for minimization. It should therefore be understood that use of the similarity measures is equivalent to use of the distances.

Claims

1. A vector quantizing method of quantizing input vectors into output codes, said vector quantizing method comprising the steps of preparing a codebook circuit (17) loaded with code vectors in accordance with codebook indexes with each code vector composed of a predetermined number of vector elements, producing at least one candidate vector of said code vectors in response to a current index selected from said codebook indexes for each of said input vectors, calculating distances between said each of input vectors and comparison vectors given by said at least one candidate vector to produce distance values representative of said distances, and evaluating said distance values to select one of said

between said codebook circuit and said distance calculator for using in said comparison vectors said at least one candidate vector as an unchanged vector without rearrangement of its vector elements and said at least one candidate vector as a rearranged vector with rearrangement of its vector elements in response to a rearrangement index, said evaluation circuit producing said selected index with no change of and with addition of said rearrangement index to said current index when said selected vector is said unchanged and said rearranged vectors, respectively.

9. A vector quantizer device as claimed in Claim 8, characterised in that said vector rearranging means comprises;

a rearrangement table circuit (23) connected to said evaluation circuit and preliminarily loaded, in accordance with table indexes, with manners of rearrangement in which each candidate vector is rearranged into said rearranged vector in one of said manners of rearrangement that is specified among said table indexes by said rearrangement index; and

a table dependent rearranging circuit (21) connected to said codebook circuit, to said distance calculator, and to said rearrangement table circuit for rearranging said at least one candidate vector into said rearranged vector in said one of manners of rearrangement.

10. A vector quantizer device as claimed in Claim 9, characterised in that:

said rearrangement table circuit is preliminarily loaded, in accordance with said table indexes and in correspondence at least to predetermined ones of said code vectors, with common manners which are selected from said manners of rearrangement so as to be common to respective parts of said predetermined ones of code vectors with each common manner selected common to a part of said predetermined ones of code vectors;

said table dependent rearranging circuit rearranging said at least one candidate vector into said rearranged vector in one of said common manners that is specified among maid table indexes by said rearrangement index when said at least one candidate vector is one of said predetermined ones of code vectors that is specified in one of said respective parts by said current index.

11. A vector quantizer device as claimed in Claim 10, characterised in that:

said vector quantizer device further comprises an input vector analyzer (27) for analyzing characteristics of each input vector to produce a result of analysis;

said rearrangement table circuit being connected to said input vector analyzer and made by said result of analysis to supply said table dependent rearranging circuit with one of said common manners that is specified in response to said result of analysis.

12. A vector quantizer device as claimed in Claim 9, each input vector representing a succession of either a consonant and a vowel or a vowel and a consonant, each code vector representing in said codebook circuit the succession of a consonant and a vowel, characterised in that:

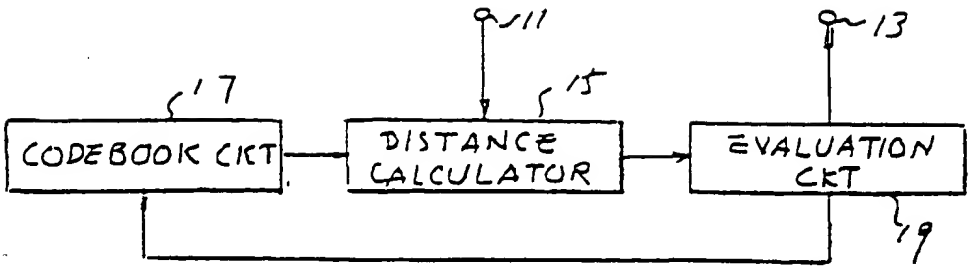
said vector quantizer device further comprises an input vector analyzer (27) for analyzing each input vector to judge whether said each of input vectors represents the succession of a consonant and a vowel or of a vowel and a consonant, said input vector analyzer producing mode zero and one signals when said input vector analyzer judges that said each of input vectors represents the succession of a consonant and a vowel and of a vowel and a consonant, respectively;

said rearrangement table circuit being connected to said input vector analyzer and made by said mode zero and one signals to be quiescent and to produce one of said manners of rearrangement in response to said rearrangement index;

said table dependent rearraning circuit using said at least one candidate vector as said unchanged vector and as said rearranged vector with said rearranged vector mode to represent the succession of the last-mentioned vowel and the last-mentioned consonant when said rearrangement table circuit is quiescent and produces the last-mentioned one of manners of rearrangement, respectively.

13. A vector quantizer device as claimed in any one of Claims 9 to 12, characterised in that said vector quantizer device further comprises a table training circuit (29) for training said rearrangement table circuit for production of said one of manners of rearrangement as an optimum manner of rearrangement in response to a plurality of training vectors which include said input vectors.

14. A vector quantizer device as claimed in Claim 8, characterised in that said vector rearranging means comprises a single rule rearranging circuit (25) connected to said distance calculator, to said codebook



Prior Art

FIG. 1

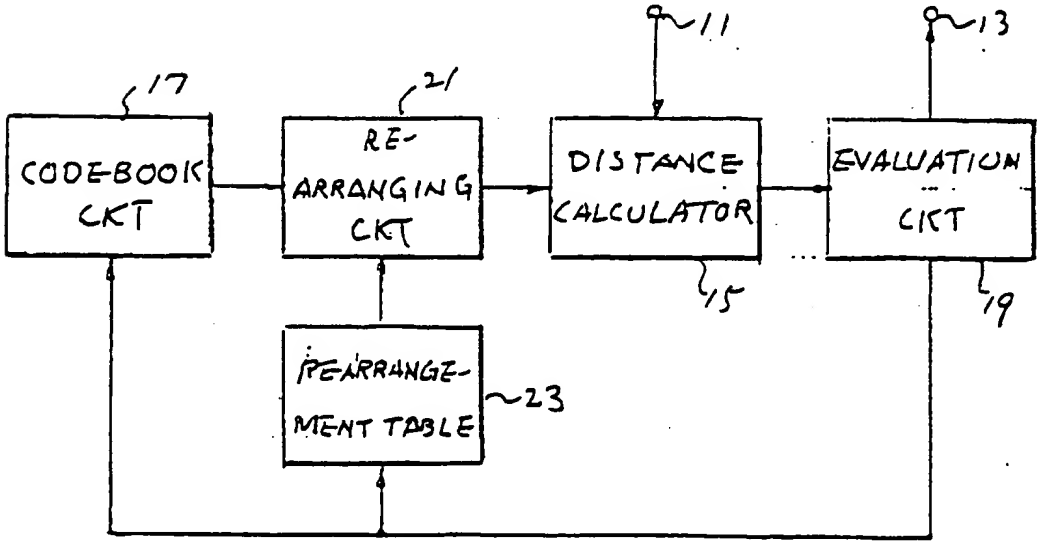


FIG. 2

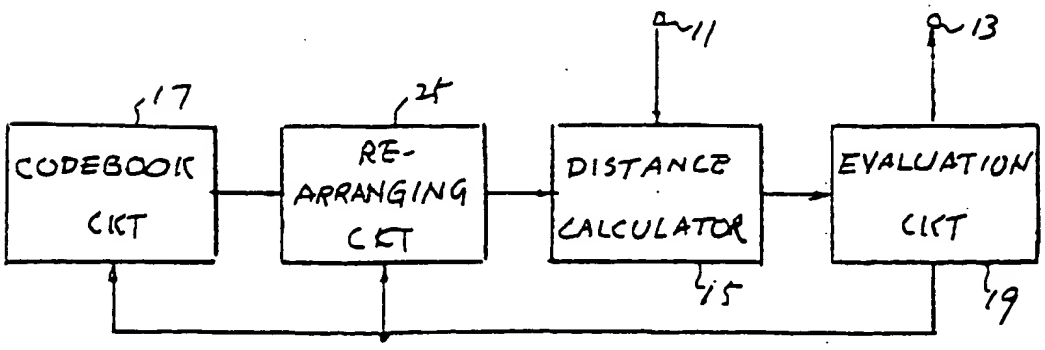


FIG. 3

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(54) Quantization of input vectors with and without rearrangement of vector elements of a candidate vector

(57) For quantizing input vectors into output codes with reference to quantization vectors with reduction of a memory capacity, a vector quantizer device comprises a rearranging unit (21, 23) between a codebook circuit (17) preliminarily loaded, in accordance with codebook indexes, with code vectors selected from the quantization vectors to produce at least one candidate vector in response to a current index and a distance calculator (15) for calculating, between each input vector and comparison vectors given by the candidade vector, distance values for supply to an evaluation circuit (19) for producing a selected index indicative of one of the comparison vectors that minimizes the distance values and for successively producing the output codes with the selected index used as each output code without or with addition of a rearrangement index. When the rearrangement index is and is not added, the rearranging circuit produces the candidate vector in each comparison vector as an unchanged vector and as a rearranged vector in which vector elements of the candidate vector are rearranged, respectively. The rearranging unit may rearrange the candidate vector in compliance with a single predetermined rule or with rules preliminarily stored in a rearrangement table circuit (23) in accordance with table indexes with one of the rules delivered to a rearranging circuit (21) in response to the rearrangement index.

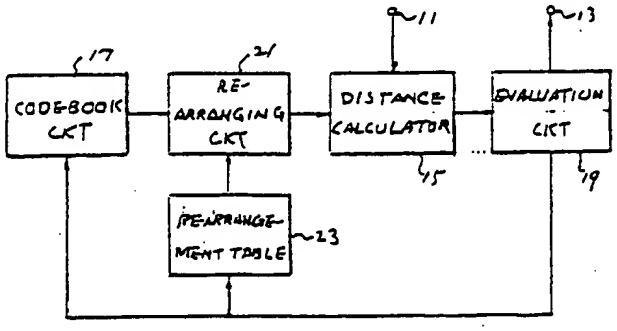

FIG. 2

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EUROPEAN SEARCH REPORT

Application Number
EP 95 10 5904

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.6)
A	US 4 959 870 A (TACHIKAWA MICHIYOSHI) 25 September 1990 * column 4, line 60 - column 5, line 9 * * column 6, line 3 - line 50 * ---	2,9	
A	PROCEEDINGS OF THE EUROPEAN CONFERENCE ON SPEECH COMMUNICATION AND TECHNOLOGY (EUROSPEECH), PARIS, SEPT. 26 - 28, 1989, vol. 2, 1 September 1989, TUBACH J P;MARIANI J J, pages 356-359, XP000210028 LIU T M ET AL: "PHONETICALLY-BASED LPC VECTOR QUANTIZATION OF HIGH QUALITY SPEECH" * abstract; figure 2 * -----	3,4,11, 12	

TECHNICAL FIELDS SEARCHED (Int.Cl.6)

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	25 June 1997	Krembel, L

CATEGORY OF CITED DOCUMENTS

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